Microcontroller-based peak current mode control using digital slope compensation

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Microcontroller Based Peak Current Mode Control Using Digital Slope Compensation

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Abstract

Microcontroller based peak current mode control of a Buck converter is investigated. The new solution uses a discrete time controller with digital slope compensation. This is implemented using only a single-chip microcontroller to achieve desirable cycle-by-cycle peak current limiting. The digital controller is implemented as a two pole, two zero linear difference equation designed using a continuous time model of the Buck converter and a discrete time transform. Subharmonic oscillations are removed with digital slope compensation using a discrete staircase ramp. A 16W hardware implementation directly compares analog and digital control. Frequency response measurements are taken and it is shown that the crossover frequency and expected phase margin of the digital control system match that of its analog counterpart.

Index Terms

Digital peak current mode control, DC-DC switch mode power supplies, discrete controller, digital slope compensation.

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NOMENCLATURE

C_O	Output filter capacitor.
D	Duty ratio.
I_O	Output current.
L_O	Output filter inductor.
Q_C	Double pole quality factor.
$Ramp$	Digital ramp height.
$Steps$	Number of digital steps per slope compensation period.
S_E	External ramp slope.
S_N	Output inductor current slope.
T_S	Switching period.
T_{SLOPE}	Digital slope compensation period.
T_{STEP}	Time taken to decrement digital ramp.
V_{DAC}	DAC voltage range.
V_{IN}	Input voltage.
V_O	Output voltage.
V_{PP}	Compensation ramp height.
m_C	Slope compensation factor.
n	Turns ratio, $n = N_S/N_P$.
n_{DAC}	Number of DAC bits.
$\Delta Ramp$	Change in digital ramp height per step.
Φ_E	Phase erosion.
Φ_M	Required open-loop phase margin.
ω_{CP0}	Compensator pole at origin.
ω_{CP1}	Compensator pole.
ω_{CZ1}	Compensator zero.
ω_N	Plant double pole.
ω_{P1}	Plant pole.
ω_{P1}	Plant zero.
ω_X	Required open-loop crossover frequency.

I. INTRODUCTION

II. REVIEW OF PEAK CURRENT MODE CONTROL

Figure 1 depicts the typical set up for analog peak current mode control of a Buck converter. The output voltage along with a reference voltage are used as inputs to an error amplifier. The capacitors and resistors in the feedback

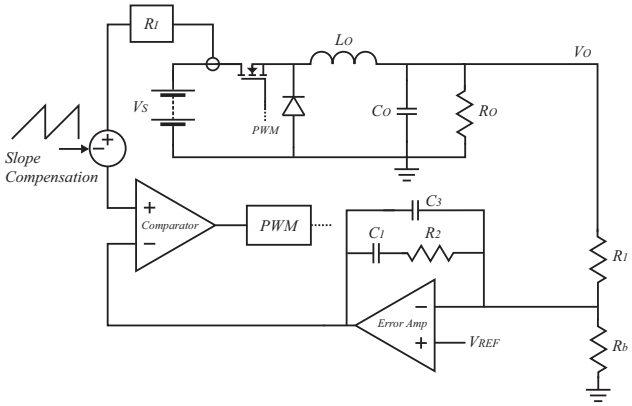


Fig. 1. Analog peak current mode control of a Buck converter.

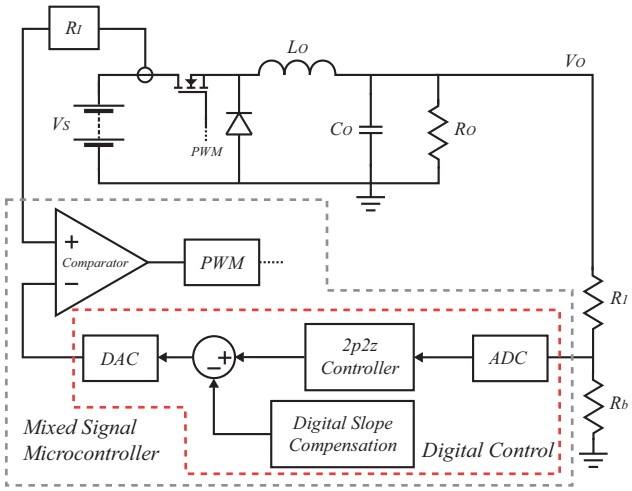


Fig. 2. Digital peak current mode control of a Buck converter.

path of the error amplifier form the poles and zeros of the compensation network. The output of the error amplifier forms the current reference voltage before slope compensation.

The peak of the output inductor current is sensed by measuring the current through the switch using either a small current sense resistor or a current transformer; both of which have an equivalent current-to-voltage gain of R_I. The sensed current is effectively a ramp; as the switch is turned on at the beginning of the pulse width modulation (PWM) period the current through it increases from its minimum to the maximum by the end of the duty period.

This sensed current is used as an input to a comparator. The second input to the comparator is the control voltage obtained from the error amplifier and compensation network. This forms the inner control loop; the current loop. Compensators can be designed for both outer and inner control loops [1], however only the outer loop is compensated in peak current mode.

When the sensed current reaches the value of the control voltage the output of the comparator changes and this

is used to trigger the end of the PWM duty cycle. Effectively the current through the inductor is limited and the plant acts as a constant current source. However, due to the voltage feedback, the converter is also able to regulate a constant voltage across a varying load.

For the digital implementation of peak current mode control presented in this paper, all of the analog control components are replaced by a single microcontroller as shown in Figure 2. Initially the PWM duty cycle is set to 100% and current is conducted through the switch. The output voltage is applied, through a sampling divider, to the ADC of the microcontroller. The analog voltage is sampled and converted to a digital value. This digital representation of the output voltage has a reference voltage (another digital value) subtracted from it and the resulting discrete time error signal is used as an input to a discrete time controller.

The capacitors and resistors of the analog compensation network are replaced by the digital coefficients of the controller. The controller design will be discussed in detail in Section VI. The output of the controller, a number, is scaled appropriately and used as an input to the microcontroller's digital-to-analog (DAC) module. This generates the current reference voltage.

The switch current is sensed using the same method as with analog control. The sensed current is used as the other input to the microcontroller's on-board comparator module with the first input supplied directly from the output of the DAC module. When the sensed current ramp reaches the control voltage the comparator's output will change. This is used as a trip inside the microcontroller to reset the PWM output and disable the switch. The result is the same operation of peak current mode control so commonly implemented in analog. Slope compensation is still required with the analog controller and this must also be implemented in digital. This will be discussed in the next Section.

III. Current Loop and Slope Compensation

An analysis of peak current mode control by Ridley in [2] determined that the subharmonic oscillations observed during peak current mode control could be represented by a double pole at half the switching frequency, F_S.

$$\omega_N = \pi F_S \tag{1}$$

The subharmonic oscillations can be removed by ensuring that the resonant peak of this double pole is sufficiently damped. The peak should be damped such that it does not cross the unity gain axis of the open loop system. This can be achieved by setting the quality factor, Q_C, of the double pole to $Q_C \leq 1$. Using this, the slope compensation factor, m_C, can be calculated. The slope compensation factor specifies the ratio of external compensation slope to output inductor slope required in order to sufficiently damp the subharmonic oscillations.

$$m_C = \frac{1 + \frac{\pi}{2}.Q_C}{\pi.Q_C.(1 - D)} \tag{2}$$

Where D is the duty cycle calculated in 3.

$$D = \frac{V_O + V_{DIODE}}{V_{IN}} \tag{3}$$

Using the slope compensation factor calculated in 2, the external ramp slope, S_E, can be found using the output inductor slope, S_N. For Buck derived topologies, the output inductor current slope during the time that the switch is on is calculated in 4.

$$S_N = \frac{(n.V_{IN}) - V_{OUT} - V_{DIODE}}{L_O}.R_I.n \tag{4}$$

$$S_E = (m_C - 1).S_N \tag{5}$$

Thus, the quality factor of the resonant peak at half the switching frequency determines the compensation ramp requirements. The required peak-to-peak value of the compensation ramp is calculated using 6.

$$V_{PP} = S_E.T_S \tag{6}$$

There is no transformer with a Buck converter and so in the above equations $n = N_S/N_P = 1$. However these equations are valid for other Buck derived topologies which include transformers; such as half or full-bridge. If a transformer is used there will be a certain amount of slope compensation provided by the magnetizing inductance of the transformer [3].

IV. Compensator Design

Using the simplified model of a PWM switch [4], an accurate model for the small-signal characteristics of peak current mode control is presented in [2] with further information in [3]. Other models are available [5] and could be investigated, however, the model in [2] is used as it performs well when compared to the hardware measurements. The subharmonic oscillations observed with peak current mode control due to small perturbations in the inductor current are predicted by this model. The compensation ramp discussed in the previous Section is added to the sensed switch current to damp these oscillations.

Many implementations take an intuitive approach to compensator design. However this paper uses an exact method to calculate the compensator poles and zeros such that the specified open loop crossover and phase margin are achieved. Using the accurate control-to-output model proposed by Ridley in [2] a Type II compensator can be analytically designed.

With peak current mode control the compensator is placed within the outer voltage loop. The inner current loop has a bandwidth of between $1/6^{th}$ and $2/3^{rds}$ of the switching frequency [6], [7]. Therefore the crossover frequency of the outer voltage loop should be less than this; between $1/20^{th}$ and $1/10^{th}$ of the switching frequency. The transfer function of the Type II compensator, given in 7, has one pole, one zero and a pole at the origin.

$$H_C(s) = \frac{\omega_{CP0}}{s} \times \frac{\left(1 + \frac{s}{\omega_{CZ1}}\right)}{\left(1 + \frac{s}{\omega_{CP1}}\right)} \tag{7}$$

The compensator pole, ω_{CP1}, is placed at the frequency of the plant's zero formed by the capacitor and its parasitic ESR.

$$\omega_{CP1} = \omega_{ESR} = \frac{1}{R_{ESR}C_O} \tag{8}$$

Intuitive placement of the compensator zero is normally used to add phase in to the open loop system around the crossover frequency. However, in this paper an exact equation is derived which analytically places the compensator zero so as to achieve the phase margin specification precisely.

At the crossover frequency, the combined control-to-output and compensator transfer functions must satisfy 9. Where ϕ_M is the required phase margin in radians and ω_X is the required crossover frequency. $H_P(j\omega)$ and $H_C(j\omega)$ are the control-to-output and controller transfer functions respectively.

$$\angle\left(H_P(j\omega_X) \times H_C(j\omega_X)\right) = -\pi + \phi_M \tag{9}$$

Through knowledge of the control-to-output transfer function as given in [2], [3] and 7, an equation for calculating the compensator zero is derived in this paper and given in 10 to precisely achieve a specified phase margin and crossover frequency concurrently.

$$\omega_{CZ1} = \frac{\omega_X}{\tan\left[\phi_V\right]} \tag{10}$$

Where:

$$\phi_V = -\frac{\pi}{2} + \phi_M + \tan^{-1}\left(\frac{\omega_X}{\omega_{P1}}\right) + \tan^{-1}\left(\frac{\omega_X}{\omega_{N1}}\right) + \tan^{-1}\left(\frac{\omega_X}{\omega_{N2}}\right) \tag{11}$$

$$\omega_{P1} = \frac{1}{R_O.C_O} + \frac{T_S}{L_O.C_O}.\left(m_C.(1-D) - 0.5\right) \tag{12}$$

$$\omega_{N1} = \frac{-\omega_N}{2.Q_C} + \sqrt{\frac{1}{Q_C^2.\omega_N^2} - 2} \tag{13}$$

$$\omega_{N2} = \frac{-\omega_N}{2.Q_C} - \sqrt{\frac{1}{Q_C^2.\omega_N^2} - 2} \tag{14}$$

In 11, the ω_{N1} and ω_{N2} terms are the complex conjugate poles of the high frequency double-pole ω_N. The inverse tangent of these pairs must be calculated accordingly. The phase contribution from ω_{CP1} negates that of ω_{ESR} and as such these terms have been omitted from 11.

Finally, the gain of the compensator can be analytically calculated to achieve the specified crossover frequency of the open loop system. This is the pole at the origin of the compensator and is the frequency at which this pole has unity gain. However, the complete open loop system should have unity gain at the specified crossover frequency. This is described in 15.

$$20\log_{10}\left[H_P\left(j\omega_X\right)\right] + 20\log_{10}\left[H_C\left(j\omega_X\right)\right] = 0 \tag{15}$$

Using the control-to-output transfer function and 7, an equation for calculating the compensator pole at the origin is given in 16 to achieve a specific crossover frequency.

$$\omega_{CP0} = \frac{\omega_X}{K_{DC} \times K_1 \times K_2} \tag{16}$$

Where:

$$K_{DC} = \frac{R_O}{n.R_I} \times \frac{1}{\left[1 + \frac{R_O.T_S}{L_O}.\left(m_C.\left(1-D\right) - 0.5\right)\right]} \tag{17}$$

$$K_1 = \frac{\sqrt{1 + \left(\frac{\omega}{\omega_{CZ1}}\right)^2}}{\sqrt{1 + \frac{\omega_X}{\omega_{P1}}^2}} \tag{18}$$

$$K_2 = \frac{1}{\sqrt{\left(1 + \frac{-\omega_X}{\omega_N^2}\right)^2 + \left(\frac{\omega_X}{\omega_N.Q_C}\right)^2}} \tag{19}$$

V. Design Example

A 16W Buck converter is designed and constructed. An input voltage of 16V and output of 8V at 2A is used. The full converter specification is given in Table Ia.

First, the slope compensation requirements are calculated given that the quality factor of the double pole at half the switching frequency is set to 1. The remaining operational parameters are calculated using the converter specification and equations presented in the previous Sections. Table Ib lists the parameters calculated for this design example.

Using the exact analytical design method presented in this paper, the compensator is designed to meet the specified phase margin and crossover frequency. For a Type II compensator, using 8, the pole is placed at the frequency of the power stage ESR zero. 10 calculates the frequency of the compensator zero required to meet the phase margin specification. Finally 16 calculates the gain of the compensator to meet the crossover specification.

The compensator poles and zeros are given in Table Ic. These exact values will be used in the next Section to design the digital controller.

This design example is simulated using MATLAB. Figure 3 depicts the theoretical frequency response of the control-to-output and controller transfer functions for the peak current mode converter design example. The controller

TABLE I

PEAK CURRENT MODE DESIGN EXAMPLE

Parameter	Value	Parameter	Value
V_{IN}	$16Vdc$	R_I	0.48
V_O	$8Vdc$	R_{ESR}	$31m\Omega$
I_O	$2A$	V_{DIODE}	$0.6V$
C_O	$440\mu F$	F_S	$200kHz$
L_O	$22\mu H$	F_X	$15kHz$
n	1	ϕ_M	$75°$

(a) Specification

Parameter	Value	Parameter	Value
Q_C	1	ω_{P1}	$732.6rad.s^{-1}$
D	0.5375	ω_{Z1}	$7.331 \times 10^4 rad.s^{-1}$
m_C	1.7693	ω_N	$6.283 \times 10^5 rad.s^{-1}$
V_{PP}	$0.621V$	K_{DC}	6.4631

(b) Operational parameters

Pole/Zero	Value
ω_{CP1}	$7.331 \times 10^4 rad.s^{-1}$
ω_{CZ1}	$1.111 \times 10^4 rad.s^{-1}$
ω_{CP0}	$2.171 \times 10^5 rad.s^{-1}$

(c) Compensator poles and zeros

has been designed using the exact method presented in this paper. The plot of the combined open loop response is stable as slope compensation is used and shows that the crossover frequency and phase margin, specified in Table Ia, are achieved precisely in the open loop system.

VI. DIGITAL CONTROLLER DESIGN

Within one switching period the microcontroller must sample the analog output voltage, convert this to a digital value, calculate the error, execute a controller based on this error and run the slope compensation algorithm using the controller output to calculate the reference current. This is then compared to the sensed inductor current in order to implement the peak current limit. When the sensed inductor current reaches the reference current a trip is set within the microcontroller and the PWM duty is disabled.

In this digital implementation the controller has been designed in the continuous time domain and will be converted

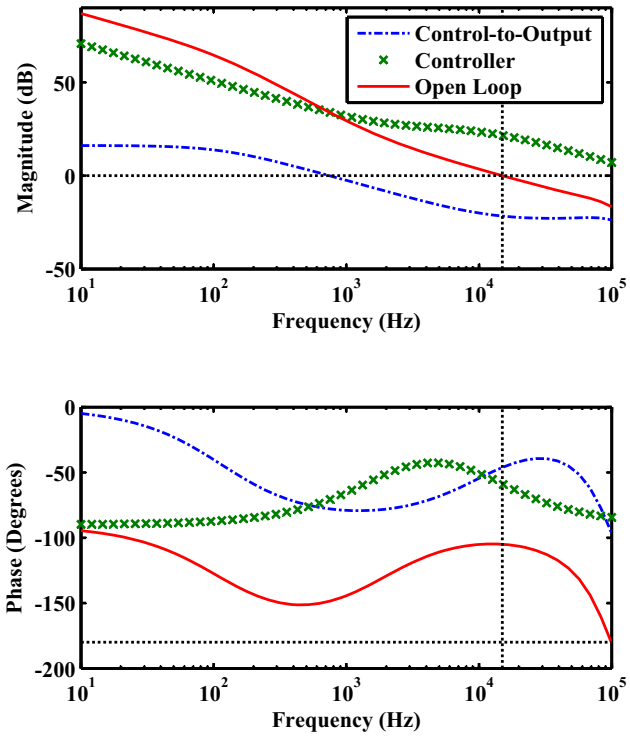


Fig. 3. Theoretical frequency response plots of the control-to-output transfer, analytically designed controller and combined open loop. Open loop crossover frequency: 15kHz, phase margin: 75°.

to the discrete time domain using the bilinear transform. The bilinear transform will be used as it provides good results up to half the switching frequency and the poles and zeros are within the unit circle [8]. Using the substitution in 20, the continuous time compensator transfer function is converted in to a discrete time transfer function in 21.

$$s = \frac{2}{T_S}\frac{z-1}{z+1} \tag{20}$$

$$H_C\left[z\right] = \frac{\omega_{CP0}}{\left(\frac{2}{T_S}\frac{z-1}{z+1}\right)} \times \frac{1+\frac{\left(\frac{2}{T_S}\frac{z-1}{z+1}\right)}{\omega_{CZ1}}}{1+\frac{\left(\frac{2}{T_S}\frac{z-1}{z+1}\right)}{\omega_{CP1}}} \tag{21}$$

After simplification, a two-pole, two-zero digital controller is derived in 22.

$$H_C\left[z\right] = \frac{B_2 z^{-2} + B_1 z^{-1} + B_0}{-A_2 z^{-2} - A_1 z^{-1} + 1} \tag{22}$$

The coefficients of the digital two-pole, two-zero controller are calculated from the compensator poles and zeros. All of the variables in these coefficients have now been defined and therefore the coefficients can be calculated analytically.

$$B_0 = \frac{T_S.\omega_{CP0}.\omega_{CP1} \times (2 + T_S.\omega_{CZ1})}{2 \times (2 + T_S.\omega_{CP1}) \times \omega_{CZ1}} \tag{23}$$

TABLE II

DESIGN EXAMPLE CONTROLLER COEFFICIENTS

Coefficient	Value
B_0	3.112327
B_1	0.168173
B_2	-2.944154
A_1	1.690211
A_2	-0.690211

$$B_1 = \frac{T_S^2.\omega_{CP0}.\omega_{CP1}}{2 + T_S.\omega_{CP1}} \tag{24}$$

$$B_2 = \frac{T_S.\omega_{CP0}.\omega_{CP1} \times (-2 + T_S.\omega_{CZ1})}{2 \times (2 + T_S.\omega_{CP1}) \times \omega_{CZ1}} \tag{25}$$

$$A_1 = \frac{4}{2 + T_S.\omega_{CP1}} \tag{26}$$

$$A_2 = \frac{-2 + T_S.\omega_{CP1}}{2 + T_S.\omega_{CP1}} \tag{27}$$

In the microcontroller, the controller is executed as a linear difference equation (LDE). This is a digital convolution algorithm. The LDE is obtained in 30 using Equations 22 and 28.

$$H_C\left[z\right] = \frac{y\left[z\right]}{x\left[z\right]} \tag{28}$$

$$y\left[n\right] \times \left(-A_2 z^{-2} - A_1 z^{-1} + 1\right) = x\left[n\right] \times \left(B_2 z^{-2} + B_1 z^{-1} + B_0\right) \tag{29}$$

$$x\left[n\right] = B_0.x\left[n\right] + B_1.x\left[n-1\right] + B_2.x\left[n-2\right] + A_1.y\left[n-1\right] + A_2.y\left[n-2\right] \tag{30}$$

Using the compensator poles and zeros in Table Ic, the numerical values for the controller coefficients are calculated in Table II using 23 to 27.

VII. DIGITAL SLOPE COMPENSATION

Under analog peak current mode, the compensating ramp is a voltage that is added to the sensed inductor current. Careful consideration is required as to the component values to ensure that enough ramp is generated in order to damp the oscillations otherwise instability will be observed.

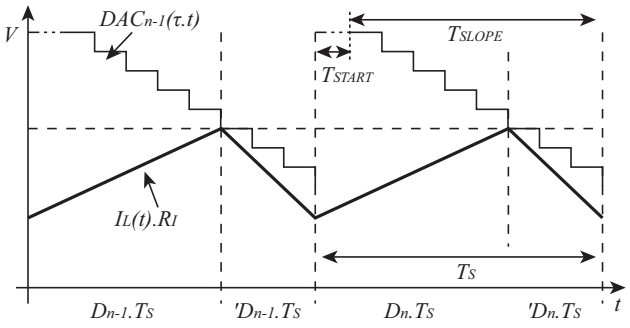


Fig. 4. Slope compensation using a digital staircase.

Under digital peak current mode, a discrete digital ramp can be subtracted from digital output of the controller at sub-intervals within the switching period. This task is particularly suited to the many microcontrollers on the market which have two or more cores. The Texas Instruments TMX320F28035 used in this example has a main core and a control law accelerator (CLA) which allows will allow the execution of both the control and slope compensation code in parallel.

The DAC connects the output of the digital controller to the input of the continuous time comparator for peak current detection. At the beginning of the switching period in Figure 4 the DAC module is loaded with the output of the digital controller; the peak current reference before slope compensation. The input to the DAC is then decremented at fixed sub-intervals throughout the switching period, simulating the compensation ramp necessary to damp any subharmonic oscillations. This digital slope compensation is in the form of a staircase with a fixed number of steps and step height over the switching period. Several parameters are defined to calculate the digital slope compensation.

$$Ramp \quad = \quad V_{PP} \times \frac{2^{n_{DAC}} - 1}{V_{DAC}} \tag{31}$$

The DAC has a specific number of bits, n_{DAC}, which represent the output voltage range, V_{DAC}. The peak-to-peak compensation ramp value, V_{PP} calculated in Section III, is converted to a discrete number using the calculation in 31. The result is the digital staircase height. The DAC resolution can be improved by setting the external DAC voltage reference pins V_{DDA} and V_{SSA}. This would be especially useful for configurations which require small values of slope compensation.

$$Steps \quad = \quad \frac{T_{SLOPE}}{T_{STEP}} \tag{32}$$

The individual number of steps and change in height per step are calculated based on the microcontroller specification. Several microcontroller instruction cycles will be required to decrement the input to the DAC for each step of the staircase type compensation. The total time for each step will be specific to the microcontroller.

TABLE III
DIGITAL SLOPE COMPENSATION PARAMETERS

Parameter	Value	Parameter	Value
V_{PP}	$0.621V$	T_{STEP}	$50ns$
n_{DAC}	$10bits$	T_{SLOPE}	$3950ns$
V_{DAC}	$3.3V$	$Steps$	79
$Ramp$	192.53	$\Delta Ramp$	-2.437

However, it is referred to as T_{STEP} for the equations herein. 32 calculates the number of discrete steps that the microcontroller can execute for one digital slope compensation period, T_{SLOPE}, within each switching period. Given this, 33 calculates the change in DAC value for each step.

$$\Delta Ramp = -\frac{Ramp}{Steps} \tag{33}$$

The digital slope compensation parameters required for the design example given in Section V are calculated in Table III. Ideally, T_{SLOPE} would be equal to the switching period. However, in practice it will take a number of time steps to begin the digital slope compensation function within each switching period, T_{START}. This is the time taken for the PWM interrupt to trigger the flushing of the pipeline and start of the CLA code execution. T_{START} has been measured as 400ns on the TI microcontroller used herein.This time is comparable to the reverse recovery time of the diode often used in the analog slope compensation circuit and forms only a small fraction of the entire duty cycle. Therefore it has no impact on the damping of subharmonic oscillations. The time step for the microcontroller used in this design example is $50ns$. The time available for slope compensation, T_{SLOPE}, is calculated as $4600ns$ as 8 time steps are required to start the slope compensation function within each switching period.

In Figure 5 the control-to-output transfer function of the hardware experimentation has been measured using a frequency analyzer in order to illustrate the effectiveness of the digital staircase slope compensation. Detailed open loop experimental results will be given in Section IX. The Figure illustrates the damping effect for different values of $\Delta Ramp$.

The first measurement taken has no digital slope compensation, $\Delta Ramp = 0$; the DAC value remains constant throughout the switching period. The characteristic resonant peak at half the switching frequency is visible. The proportional gain had to be reduced such that the resonant peak did not cross the unity gain axis; allowing stable operation and a frequency response measurement to be obtained. This does not change the shape of the magnitude plot.

The remaining measurements are taken with digital slope compensation applied using varying values of $\Delta Ramp$. As expected, damping of the resonant peak increases as the digital compensation ramp is increased. When $\Delta Ramp$

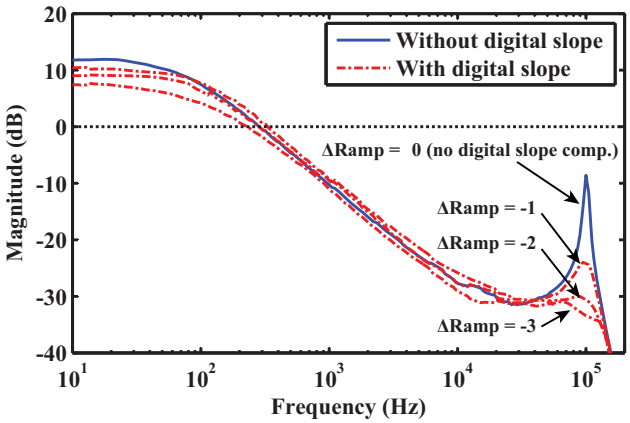


Fig. 5. Measured control-to-output frequency response using an OMICRON Lab Bode 100 network analyzer comparing with and without digital slope compensation for varying $\Delta Ramp$ values.

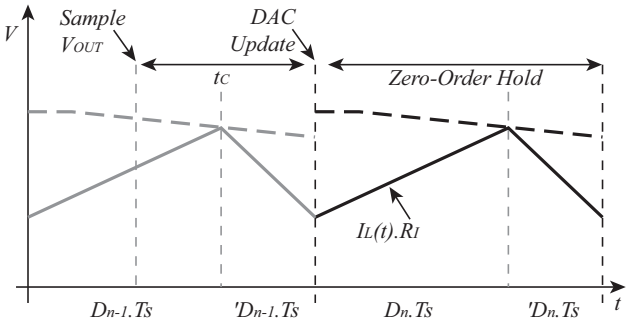


Fig. 6. Time delays introduced with a digital controller. t_c is the time spent sampling and performing calculations within the controler.

is between -2 and -3, the resonant peak is sufficiently damped and the converter operation is stable with the proportional gain returned to the correct value. This indicates that the novel digital staircase implementation of slope compensation achieves the same damping effect as analog slope compensation.

VIII. Phase Erosion

With digital control, care must be taken to calculate the sources of delay within the system. These delays manifests themselves as a phase margin erosion that is significant for high crossover frequencies. Therefore, with digital control it is necessary to calculate these delays and ensure that the compensator is designed to allow for this phase erosion.

Two factors contribute to phase erosion; the phase delay due to the sampling and calculation time [9], ϕ_{CALC}, and the phase delay due to the zero-order hold, ϕ_{ZOH}. The sampling and calculation time begins when the output voltage is sampled and ends when the LDE output has been calculated and is ready to be used. The output voltage is sampled and the controller value is calculated in one period and the output of this is used in the following period. Therefore, as illustrated in Figure 6, the sampling point should be as near to the end of the switching period as

possible in order to minimize this delay. Furthermore, it is up to the designer to write efficient code which minimizes the time spent performing calculations. Ideally, the output voltage is sampled in one period and the output of the controller is ready just before the beginning of the next period taking a total time t_C.

The controller output remains fixed for the duration of the following switching period. This zero-order hold introduces a time delay of half the switching period, T_S [10]. The total time delay is the sum of the sampling and calculation delay and the delay introduced by the zero-order hold. However, the sampled data analysis used to derive the peak current mode model by Ridley in [2] already includes the effects of the zero-order hold. Therefore, when using this particular peak current mode model, only the sampling and calculation delay need be considered.

$$\phi_E = \phi_{CALC} + \phi_{ZOH} \tag{34}$$

$$\phi_{CALC} = 360^\circ \times F_X \times t_C \tag{35}$$

$$\phi_{ZOH} = 360^\circ \times F_X \times \frac{T_S}{2} \tag{36}$$

For digital peak current mode using this model $\phi_{ZOH} = 0$. The required phase margin has already been specified as $\phi_M = 75^\circ$. The stability of the digital controller must be considered after phase erosion. In this case, the phase erosion is caused by the delay between sampling and update of the DAC value only. This hardware and software dependent time can be measured either by counting the number of instructions executed or by toggling an output pin at the appropriate intervals. For this design example, the sampling and calculation time has been measured as $2.35\mu s$ by toggling an output pin as sampling begins and as the controller calculation ends. The expected phase erosion is calculated in 37.

$$\begin{aligned} \phi_E &= 360^\circ \times F_X \times t_C \\ &= 360^\circ \times \left(15 \times 10^3\right) \times \left(2.35 \times 10^{-6}\right) \\ &= 12.69^\circ \end{aligned} \tag{37}$$

$$\therefore$$

$$\phi_D = \phi_M - \phi_E = 62.31^\circ \tag{38}$$

The expected phase margin of the digital open loop system after phase erosion, 38, is still sufficiently large allowing stable operation as the analog converter was purposely designed with a good phase margin of 75°.

IX. Experimental Results

The hardware experimentation shown in Figure 7 uses a common power stage with connectable analog and digital control boards to ensure an exact comparison between the two domains. The component values of the compensation

Fig. 7. Peak current mode Buck converter with 16W load (bottom right), analog control board (top right) and digital control board (left).

network on the analog controller board are calculated from the compensator poles and zeros given in Table Ic. The analog board is populated with component values nearest to those calculated for the Type II error amplifier.

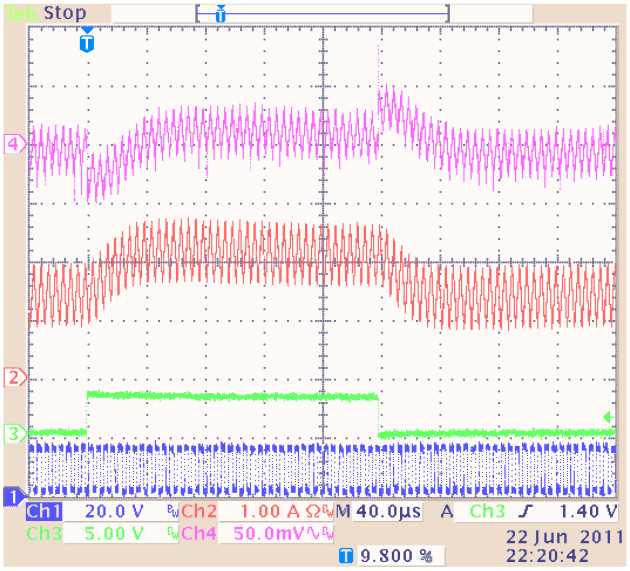
The digital system is implemented using a Texas Instruments TMX320F28035 microcontroller and the precise controller coefficients required are entered in software. This microcontroller was chosen because of its on-board comparator, DAC and CLA modules. The CLA allows the digital slope compensation code to be executed in parallel to the main controller. For the power stage, a Texas Instruments UCC27200 high side driver is used to drive an IRFR3708PBF N-channel MOSFET.

Both control schemes result in stable steady state operation for varying loads. Oscilloscope plots of the transient response of the analog and digital control methods under continuous conduction mode (CCM) are given in Figures 8 and 9 respectively. The tests are performed as the load is switched from 67% to 100% and vice versa. Automatic switching of the load in and out of the circuit is performed by a low side MOSFET.

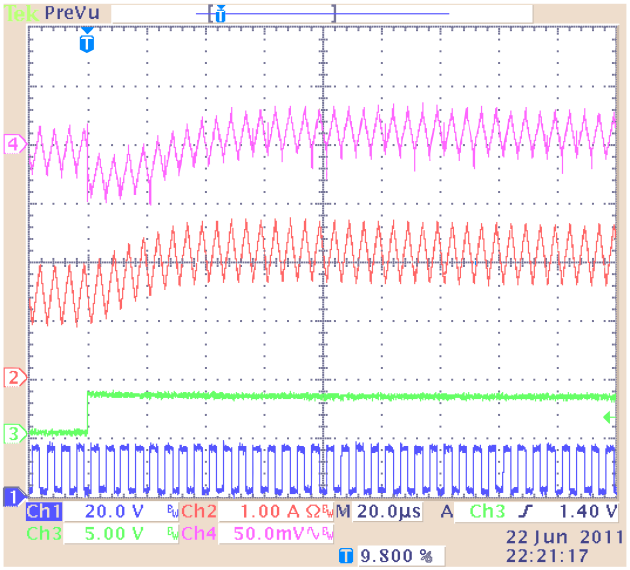
The output voltage (Ch4) is AC coupled and shows the controller's response to a step change in load (Ch3). The repetitive sawtooth shape of the output voltage is due to the product of the AC component of the output current and the capacitor's parasitic ESR. The transient response measurements should therefore be taken as the average of this waveform over each switching cycle. The inductor current (Ch2) of the analog and digital systems can be clearly seen in Figures 8b and 9b respectively. The effective regulation of the peak current by the digital controller as the load changes is shown. The digital response in Figure 9b is almost identical to the analog response in Figure 8b.

The transient responses in Figures 8 and 9 both show a stable overdamped response with a settling time of approximately $80\mu s$ and less than $50mV$ overshoot. The overdamped response is indicative of a good phase margin. The digital transient response in Figure 9 is marginally better than the analog counterpart as the digital system has a lower phase margin. This is due to the phase margin erosion discussed earlier.

Under discontinuous conduction mode (DCM) the control-to-output transfer function of the peak current mode converter changes [11]. The controller has been designed to meet the crossover and phase margin specifications for



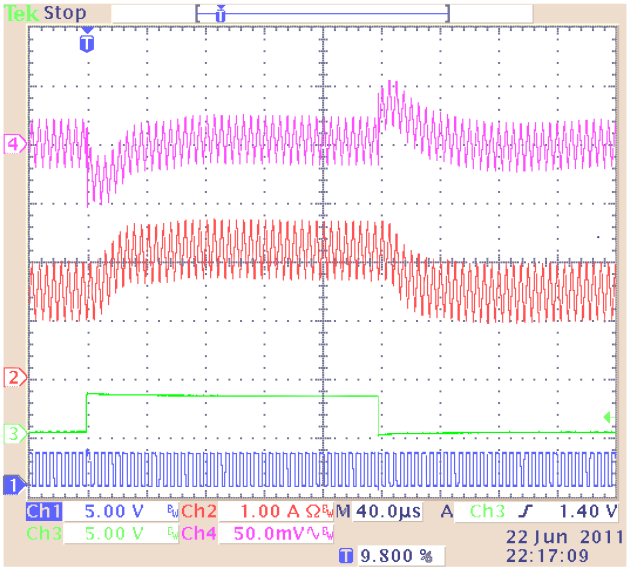
(a) Measured transient response of analog system.



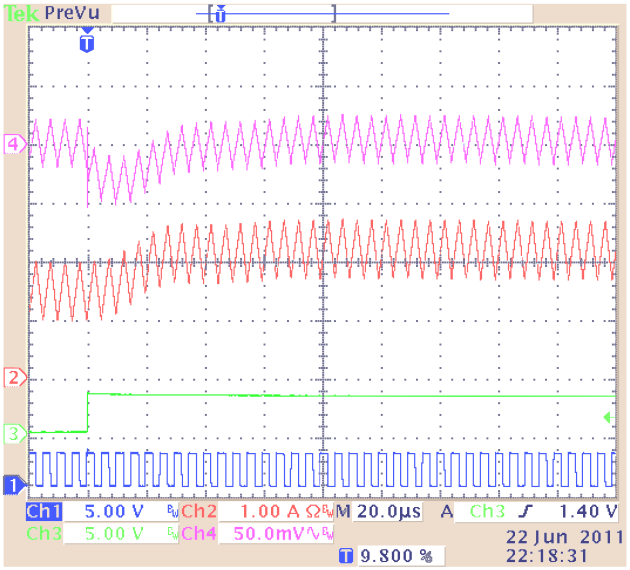
(b) Close-up view of analog system transient response.

Fig. 8. Measured continuous conduction mode (CCM) transient response of the analog system using Tektronix TDS3014B as load is switched from 67% (6Ω) to 100% (4Ω) and vice versa. Ch1: Switch PWM. Ch2: Output inductor current. Ch3: Load switching (high: 100%, low: 67% load). Ch4: AC coupled output voltage.

CCM only. However it is prudent to check the transient response of the converter when operating in both CCM and DCM modes to ensure stability and speed of response. The transient response of both analog and digital control methods under DCM operation is shown in Figures 10a and 10b. The response is stable as the load is switched from 1% to 10% and vice versa. The settling time under DCM has increased to approximately $300\mu s$, due to the change in control-to-output model, with the overshoot remaining less than $50mV$.



(a) Measured transient response of digital system.

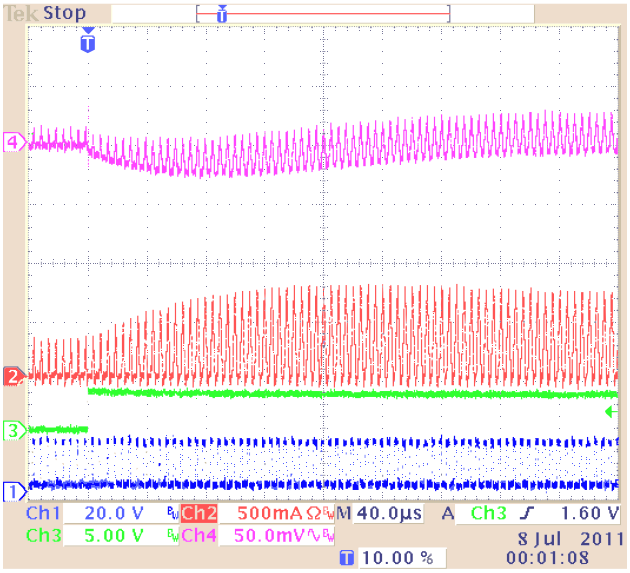


(b) Close-up view of digital system transient response.

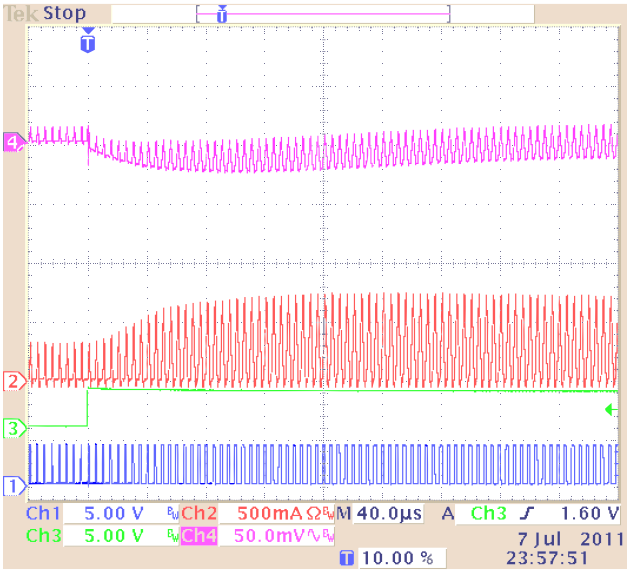
Fig. 9. Measured continuous conduction mode (CCM) transient response of the digital system using Tektronix TDS3014B as load is switched from 67% (6Ω) to 100% (4Ω) and vice versa. Ch1: Switch PWM. Ch2: Output inductor current. Ch3: Load switching (high: 100%, low: 67% load). Ch4: AC coupled output voltage.

From the Figures, under both CCM and DCM, it can be seen that the behavior of the novel digital peak current mode controller is equivalent to its analog counterpart as both control schemes show a similar response to the stepped change in load.

To further confirm the suitability of the proposed digital scheme, frequency domain analysis is used. The open loop frequency response of the converter is measured in Figure 11 using an OMICRON Lab Bode 100 vector



(a) Measured transient response of analog system.



(b) Measured transient response of digital system.

Fig. 10. Measured discontinuous conduction mode (DCM) transient response using Tektronix TDS3014B as load is switched from 1% (330Ω) to 10% (38Ω).

network analyzer. Both analog and digital control methods have a 15kHz crossover frequency for fast transient response. The measured analog phase margin of 76° matches the design specification and the lower digital phase margin of 58° is due to the phase margin erosion. The expected digital phase margin after phase erosion calculated in 38 was 62°. The difference would be due to any additional delays unaccounted for within the system.

The deviations from the theoretical results at the lower frequencies are expected. In order to achieve the high crossover frequency a large gain is required. However, in reality the gain bandwidth product of the error amplifier

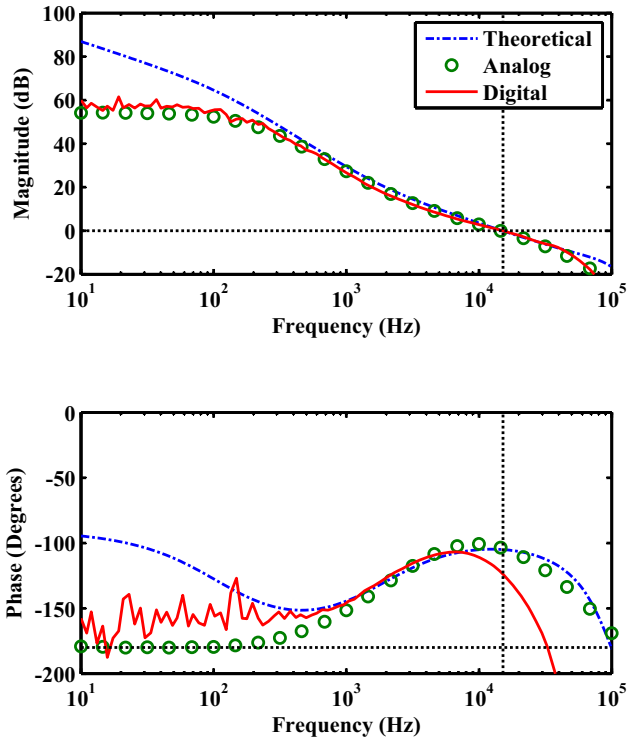


Fig. 11. Measured open loop frequency response at full load, 16W, using an OMICRON Lab Bode 100 vector network analyzer. Crossover frequency/phase margin: Analog 15kHz, 76°. Digital 15kHz, 58°.

used in the analog design will limit this gain. As the frequency increases, and the required gain reduces, the amplifier re-enters its linear region.

An analogous effect occurs in the digital domain. Quantization errors occur in both the ADC and DAC. Furthermore, the microcontroller has a 32-bit word length and uses fixed point arithmetic resulting in additional quantization during calculations. This, combined with the limited output range of the DAC, has the effect of limiting the low frequency gain; similar to the gain bandwidth product limitation of the analog domain. This can result in limit cycling if the microcontroller modules have insufficient resolution [12]. Therefore it is necessary to calculate the minimum number of bits required for ADC, DAC (or DPWM) modules before selecting the appropriate microcontroller [13], [14]. The results obtained during this experiment show that, in both systems, the low frequency gain is sufficiently large for this not to be an issue.

The controller is coded such that an output pin is toggled when the subroutine starts and finishes. Figure 12 plots the duration of the controller subroutine against the switching period. The controller occupies 26% of the switching period leaving 74% of the MCU available to perform other tasks. As discussed in the introduction, this could include running multiple converters, communications, condition monitoring and a user interface. This presents a clear advantage over analog control in systems where a microcontroller is already used. Given sufficient bandwidth, the analog control components could be removed and this task would be performed by the microcontroller already

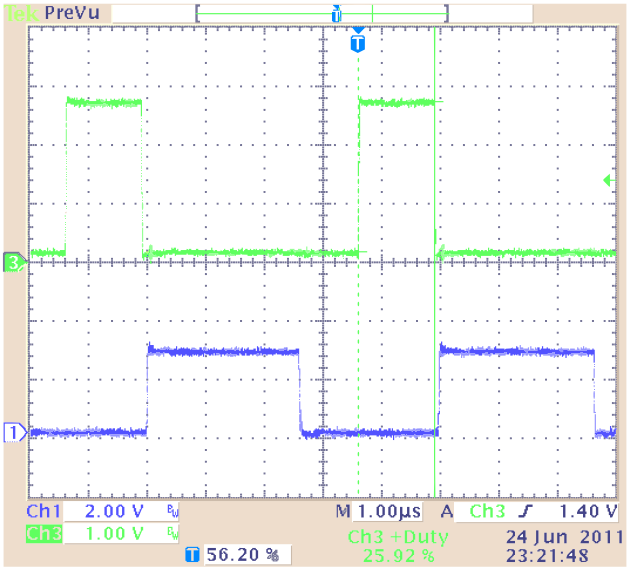


Fig. 12. Digital controller subroutine execution time vs. the switching period. Controller occupies less than 26% of MCU bandwidth. Ch1: Switch PWM. Ch3: Toggle of output pin indicating controller start/finish.

within the system; reducing the overall cost of the design and increasing the flexibility.

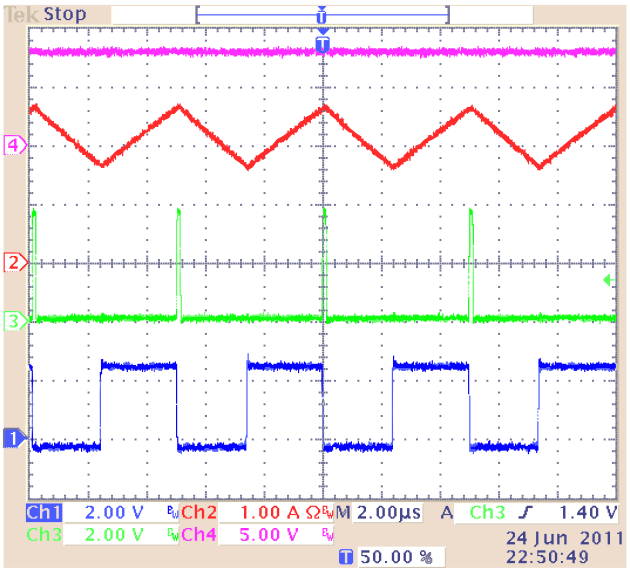


Fig. 13. Steady state waveforms at 100% load. Ch1: Switch PWM. Ch2: Output inductor current. Ch3: Comparator output (PWM module trip input). Ch4: Output voltage.

Finally, the steady state operation of the converter is shown in Figure 13. The DAC and slope compensation modules are internal to the microcontroller and set in software. Thus, these cannot be included on the oscilloscope plot. However the output of the peak current detection comparator is available (Ch3) and marks the end of the

PWM duty cycle (Ch1) as the switch current has reached the reference value set by the controller. The duty at full load is 51% and no subharmonic oscillations are observed.

Figure 5 in Section VII measures the control-to-output transfer function of the hardware converter with varying degrees of digital slope compensation. For the case where no digital slope compensation is added, $\Delta Ramp = 0$, the system is unstable as subharmonic oscillations are observed. The resonant peak at half the switching frequency is clearly underdamped. In the hardware experimentations presented in this Section, the digital slope compensation method is used and the system is stable. This indicates that the novel digital staircase slope compensation method presented in this paper is effective.

X. Conclusion

A new method of implementing peak current mode control using a discrete time controller, digital staircase slope compensation and a mixed signal comparator has been described which enables cycle-by-cycle current limiting and therefore true peak current mode operation.

Using established continuous time domain models [2], the compensator poles and zeros are analytically calculated in the continuous time domain and converted in to the discrete time domain using the bilinear transform. The discrete time two pole, two zero controller is implemented as a linear difference equation within the microcontroller.

A novel digital staircase ramp is used to implement the digital slope compensation required to damp subharmonic oscillations. Experimental measurements indicate that the digital staircase has the same effect as analog slope compensation and is accurately able to remove the resonant peak at half the switching frequency. Furthermore, the control-to-output transfer function is measured with and without digital slope compensation. The measurement indicates that the system will be unstable without the digital slope compensation and stable when the compensation is added. Thus, the effectiveness of this compensation scheme is shown. Equations are given to calculate the ramp parameters to implement this effective method of digital slope compensation.

Frequency response measurements confirm that the converter using digital control is able to match the performance of the converter using analog control in terms of a high crossover frequency and good phase margin for this design specification.

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