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A Double Data Rate (DDR) Architecture for OFDM Based Wireless Consumer Devices

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***Abstract*—The creation of OFDM based Wireless Personal Area Networks (WPANs) has allowed high bit-rate wireless communication devices suitable for streaming High Definition video between consumer products as demonstrated in Wireless-USB. However, these devices need high clock rates, particularly for the OFDM sections resulting in high silicon cost and high electrical power. Acknowledging that electrical power in wireless consumer devices is more critical than the number of implemented logic gates, this paper presents a Double Data Rate (DDR) architecture to reduce the OFDM input and output clock rate by a factor of 2. The architecture has been implemented and tested for Wireless-USB (ECMA-368) resulting in a maximum clock of 264MHz instead of 528MHz existing anywhere on the die.**

I. INTRODUCTION

Recently Ultra-Wideband (UWB) systems were proposed to standardize high bandwidth wireless communication systems, particularly for Wireless Personal Area Networks (WPAN). The fundamental issue of UWB is that the transmitted signal can be spread over an extremely large bandwidth with a very low Power Spectral Density (PSD). In 2002, the Federal Communications Commission (FCC) agreed to allocate 7500 MHz spectrum in the 3.1-10.6 GHz band for unlicensed use for UWB devices [1] and limited the UWB Effective Isotropic Radiated Power (EIRP) to -41.3dBm/MHz [2].

In 2005 the WiMedia Alliance [3] working with the European Computer Manufacturers Association (ECMA) announced the establishment of the WiMedia MB-OFDM (Multiband Orthogonal Frequency Division Multiplexing) UWB radio platform as their global UWB standard, ECMA-368. ECMA-368 was also chosen as physical layer (PHY) of high data rate wireless specifications for high-speed Wireless USB (W-USB) [4], Bluetooth 3.0 [5] and Wireless High-Definition Media Interface (HDMI) [6]. Recently ECMA-368 has published a second updated version [7].

At the heart of ECMA-368 lies a 128-pt FFT with a 242.42ns FFT period resulting in each FFT bin being clocked at 528MHz. Each OFDM is separated with a Zero Padded Suffix (ZPS) of 70.08ns (37 zeros). Although 528MHz is within the realm of today's System on Chip (SoC) capability, the high clock rate can cause interference, layout issues and large electrical power issues. Prototyping at 528MHz is still difficult with today's technology and even the latest Field Programmable Gate Arrays (FPGAs) tend to have a maximum of 500MHz even for local clocks.

This paper presents a Double Data Rate (DDR) architecture for Wireless OFDM consumer devices by parallelizing the transmit and/or the receive paths into two processing paths, each clocking at half the output rate of 264MHz. The transmit paths are buffered, merged together and output with odd and even values on each clock edge as supported by modern Analogue to Digital Converters (ADCs). The receive path DDR is split into two after the reception of the DDR data from the Digital to Analogue Converters (DACs) and are merged just after equalization.

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II. DDR ARCHITECTURE

A. Transmit path

Figure 1 presents the architecture of the transmit path. The Interleaver operates on a block of bits to be interleaved, and outputs the interleaved result. However, where the Interleaver output would normally be applied to the Mapper (QPSK, 16-QAM, DCM, etc), in this case the Interleaver output is split into blocks of lengths suitable for each OFDM. The first block is passed to the upper path and the upper Mapper, while the next block is passed to the lower path. However, the clock rates for each path is half that of the conventional one path architecture because the same throughput occurs. Each Mapper drives its following IFFT to create each successive OFDM at half the output rate, in an even and odd fashion. Each IFFT output is sent to a Buffer consisting of 2 parallel blocks of internal memory. The IFFT output is sent to both blocks of memory to linear increasing addresses (0, 1, 2,..). When the Buffer is full, the values from even addresses (0, 2, 4,…) from one of the blocks of memory is read while at the same time the values from only the odd addresses (1, 3, 5,…) from the other block of memory is read creating both odd and even outputs on the same clock, while emptying the Buffer at twice the arrival rate. As both the blocks of memory evacuate at twice the arrival rate then the output from the blocks of memory occur at guaranteed different times from each other, hence a simple multiplexing operation occurs (simple synchronization can be applied to read the Buffer at specific times if needed.) The odd and even multiplexed transmit complex symbols are then applied to Double Date Rate Registers such that the even symbol is output on one edge of the clock and the odd symbol on the other edge, creating two output symbols per clock cycle at half the natural OFDM rate. Although it is logical to incorporate a DAC onto the System on Chip (SoC), our system outputs Low Voltage Differential

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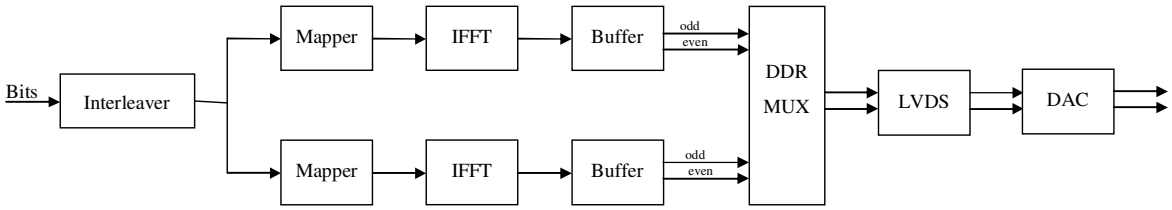

Fig. 1. Transmit chain DDR Architecture.

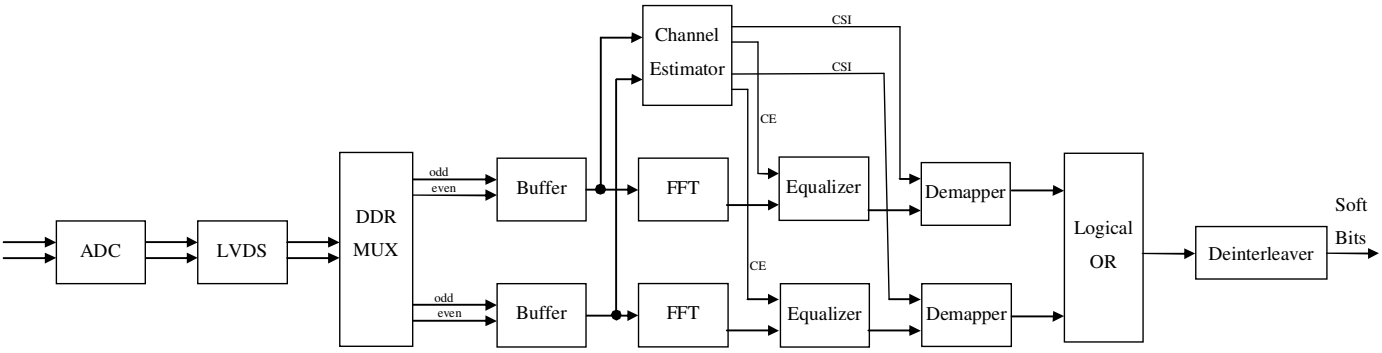

Fig. 2. Receive chain DDR Architecture.

Signaling (LVDS) levels to interface to common high speed LVDS DDR DACs.

B. *Receive path*

Figure 2 presents the receive path. The received LVDS DDR signals are collected into blocks of FFT width and split into two paths. Each path starts with a Buffer to capture the odd and even signals and then to output a single stream of symbols for the following FFT. The FFT feeds the Equalizer in the conventional way. Of note is that due to two Equalizers being present, the channel estimate for both paths is required at the same time and in our system this is achieved by having a Channel Estimator with two dedicated output ports (using two sets of dual-port RAM) to supply the channel estimate for each Equalizer. The equalized symbols are applied to the Demapper (QPSK, 16-QAM, DCM, etc) creating soft-bits with the aid of the Channel State Information (CSI) [8], again derived from dedicated outputs from the Channel Estimator. In our case, the OFDM received symbols arrive in sequence, and as each path is identical and deterministic, then the output from each Demapper occurs at guaranteed different times, so the Demapper outputs are merged into one path with a simple logical OR. In the case where this cannot be guaranteed, a local synchronized buffer will suffice. The result is a single bus of soft-bits applied to the Deinterleaver.

III. Implementation and Results

The transmitter and receiver were implemented in Verilog 2001 and successfully synthesized and implemented in a modern FPGA. The FPGA has 2 input clocks, one of 100MHz to drive a local soft-processor while a second input clock of 66MHz drives a local clock manager which multiplies the input clock by 4 creating 264MHz, that being half the natural FFT rate. The 264MHz clock drives the main logic including the main modules, FFTs, Buffers and also the input/output DDR registers. The use of LVDS buffers allows the interfacing of external LVDS DDR ADC's and DAC's for prototyping.

IV. Conclusions

Many modern consumer devices are expected to handle large amounts of data through a fast wireless connection; however this need places large demands on system clock rates and silicon performance. This paper has presented a tested and implemented mechanism to reduce the clock rates by a factor of two utilizing two parallel symbol processing paths. Although this application has been for ECMA-368, the technology is applicable to any OFDM based system.

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