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A two-dimensional RC network topology for fault-tolerant design of analog circuits

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Abstract: This paper proposes a novel one-port passive circuit topology consisting of a two-dimensional network of resistors and capacitors, which can be used as a fault-tolerant building block for analog circuit design. Through an analytical procedure, the network is shown to follow simple first-order admittance dynamics. A Monte Carlo method is employed to describe the effect of simultaneous faults (short or open circuit) in random network elements in terms of confidence bounds in the frequency-domain admittance profile. Faults in 10 % of the elements resulted in only minor changes of the frequency response (up to 3.9 dB in magnitude and 12.5 degrees in phase in 95 % of the cases). An example is presented to illustrate the use of the proposed RC network in the fault-tolerant design of a low-pass filter.

Keywords: Fault-tolerant circuits, RC networks, Fault resilience, Filter design.

1 Introduction

Faults arising from mechanical stress, temperature variations, power surges and general aging have long been causes of concern in the life cycle of electronic equipment. However, with components now reaching molecular-scale dimensions and power density levels ever increasing, fault tolerance has become an even more important aspect in the design of integrated circuits [1]. This is a crucial issue for devices operating under harsh environmental conditions, especially those exposed to high-energy particles or x-ray and gamma radiation, such as satellite and space exploration vehicles [2], robotic systems for nuclear waste disposal [3], and detector circuits for high-energy physics experiments [4]. In this case, the effects may range from soft errors to full system failures after long-term exposure [5]. Faults may also be caused by imperfections in the manufacturing process, even in advanced devices such as quantum-dot cellular automata (QCA) [6], which have been prone to cell misplacement problems [7], [8].

Fault-tolerant designs usually exploit one or more redundancy techniques, either in the physical or logical levels [3], [9]. Different configurations can be exploited to achieve larger reliability at the expense of additional power consumption, area overhead or reduction in performance [1]. It may be possible, e.g. to identify critical gates according to the impact that a fault would cause on the overall circuit output and then prioritize the hardening of these gates in the trade-off between reliability and area overhead [10]. Dual and triple-modular redundancy techniques with different voting designs have also been extensively employed [11]. As an alternative, reduced-precision redundancy techniques have been proposed to reduce the design overhead in applications such as image and video processing, which tolerate some degrading in the precision of the results [12].

Faults can also be an issue in analog circuits [13], such as phase-locked loops [14] and delay-locked loops [15]. In this case, fault-tolerant design may be even more challenging compared to digital architectures, owing to the need to choose suitable component types and component values [16]. A critical issue consists in avoiding single points of failure, so that the failure in any component leads to minimal performance degradation [17]. It is worth noting that simply duplicating circuit modules and combining their outputs may not provide a satisfactory solution, since the combination circuit itself becomes a single point of failure. Within this scope, adopting a suitable circuit topology is of foremost importance [18], [19].

The present paper presents a circuit topology consisting in a planar array of resistive and capacitive elements with no single point of failure. The ordered structure of this array is similar to 2D structures with periodic blocks that have been used in materials science to study the properties of some types of metamaterials [20]. However, to the best of the authors' knowledge, this type of topology has not been exploited for the purpose of fault-tolerant circuit design.

For illustration, a low-pass filter is designed in order to meet given specifications even in the presence of multiple component faults.

2 Proposed topology

Figure 1 presents the proposed topology for the RC circuit, which consists of n rows and n columns of four-resistor cells linked by capacitors. The terminal nodes are indicated by A and B. The circuit components amount to $4n^2$ resistors and $n(2n-1)$ capacitors, with individual resistance and capacitance values denoted by R and C, respectively. Different filters can be designed by using the proposed circuit as a building block. The inset in Fig. 1 presents a low-pass filter configuration.

The proposed topology can be assembled in either planar or cylindrical shape, with longitudinal axis oriented from points A to B. Interestingly, the circular symmetry about the A-B axis and the repetition of the same pattern of resistors and capacitors across the n rows leads to a simple expression for the admittance of the circuit. Indeed, let v_{AB} and i denote the voltage across the circuit terminals and the input current, as illustrated in Fig. 2a. Owing to the symmetry of the circuit, the current flowing into each of the n topmost branches is i/n. This current splits into two halves $i/(2n)$ at the top of a resistive cell and again becomes i/n at the bottom of the cell, as shown in Fig. 2b. It follows that the overall current-voltage relationship of the circuit in the Laplace domain is given by

$$V_{AB}(s) = 2nR\frac{I(s)}{2n} + (n-1)\frac{I(s)/n}{sC} = \left(R + \frac{n-1}{nsC}\right) I(s) \Rightarrow Y(s) = \frac{I(s)}{V_{AB}(s)} = \frac{nsC}{nsRC + n - 1} \tag{1}$$

As can be seen, the admittance $Y(s)$ is given by a simple first-order expression, which is convenient for design procedures. For large n, the admittance can be approximated as $Y(s) \simeq sC/(sRC+1)$. This expression becomes exact if an additional row with n capacitors is included at the top or bottom part of the circuit.

Under nominal operating conditions (i.e. in the absence of faults), the resistive cells at each row of the circuit lie at the same potential level. Therefore, no currents flow through the lateral capacitors linking those cells. However, these capacitors provide alternative current paths when faults occur.

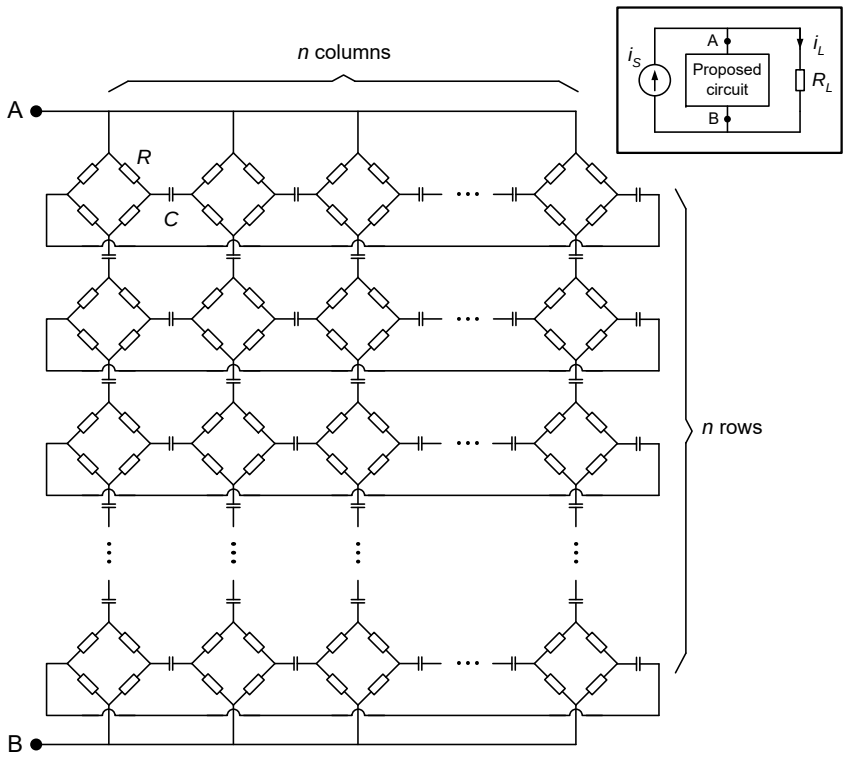

Figure 1: Proposed circuit topology. The inset shows a low-pass filter configuration with a load of resistance R_L.

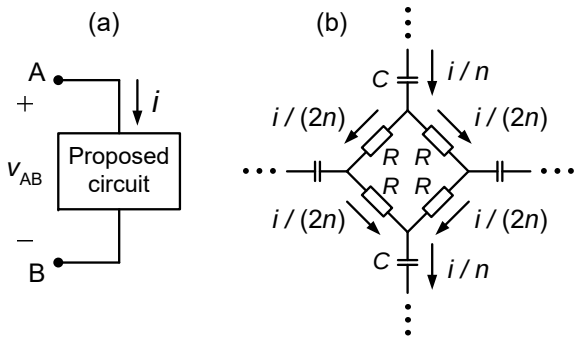

Figure 2: (a) Proposed circuit with input current and voltage denoted by i and v_{AB}, respectively. (b) Symmetrical distribution of currents within each cell of resistors.

3 Modelling the effect of faults

Herein, a method is proposed to model the effect of possible faults in the admittance of the circuit. For this purpose, initial assumptions are required on the nature of the faults (short and/or open circuit in the resistors and/or capacitors) and their extent (fraction of the affected components). A Monte Carlo simulation is then carried out by randomizing the location of the faulty components and obtaining the resulting admittance values for a prototype circuit with unit resistance and capacitance values. To this end, a MATLAB® code was developed to build a spice

netlist for the faulty circuit and convert it to incidence matrix form, which was then employed in the computational modelling procedure described in previous work [21]. Finally, the $\alpha/2$ and $(1-\alpha/2)$ quantiles of the amplitude and phase are determined at each frequency f, for a given choice of $\alpha \in [0,1]$. From the prototype admittance $Y_p(j2\pi f)$, the admittance of a circuit with non-unit R, C values is given by $Y(j2\pi f) = R^{-1}Y_p(j2\pi fRC)$.

For illustration, consider a prototype circuit with $n = 5$, which is comprised of 100 resistors and 45 capacitors. The Monte Carlo simulation was performed by introducing faults in 10 % of the components (10 resistors and 5 capacitors), with equal probabilities of short or open circuit in each component. A short (open) fault in an individual resistor was simulated by reducing (increasing) its resistance value by a factor of 10^3. In an individual capacitor, the capacitance value was increased (reduced) by the same factor for short (open) faults. The results of 1000 Monte Carlo runs are presented in Figure 3. The solid black line corresponds to the nominal admittance values, i.e. without faults. The dashed black lines are the lower and upper quantiles obtained for $\alpha = 0.05$. As can be seen, in 95 % of the cases, the faults resulted in only minor changes of the frequency response (up to 3.9 dB in magnitude and 12.5° in phase). Moreover, in none of the simulations a complete failure of the circuit (i.e. a short or open between nodes A, B) was observed.

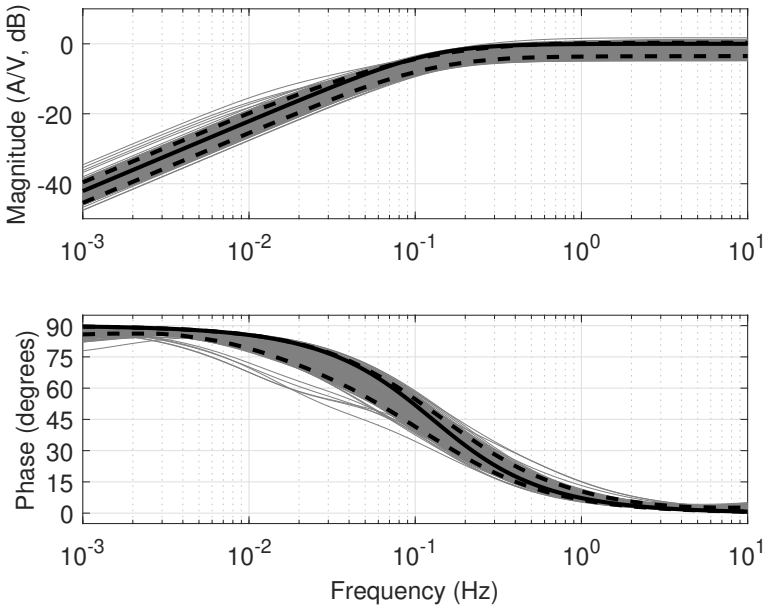

Figure 3: Monte Carlo simulation results of a prototype circuit with faults (1000 runs). The solid and dashed black lines correspond to the nominal admittance values (i.e. without faults) and the 2.5 %, 97.5 % quantiles.

Remark: At low and high frequencies, the circuit tends to purely capacitive and resistive behaviour, respectively. In the nominal case, the equivalent capacitance and resistance values are $C_{eq} = nC/(n-1)$ and $R_{eq} = R$, as can be seen from the admittance expression in (1). For the prototype circuit with $n = 5$, these values are $C_{eq} = 1.25$ and $R_{eq} = 1$ (normalized units). By using the Monte Carlo results presented in Fig. 3, the estimated values for C_{eq} and R_{eq} in the presence of faults lie in the intervals $C_{eq} \in [0.85, 1.66]$ and $R_{eq} \in [0.96, 1.49]$ in 95 % of the cases. If the circuit is to be employed in a frequency range where the admittance is mainly capacitive or resistive, these confidence intervals can be used in standard tolerance design methods [22].

In what follows, an example will be presented to illustrate the use of the amplitude and phase quantiles for fault tolerant design of a low-pass filter.

4 Fault-tolerant design example

Assume that a low-pass filter is to be designed as in Fig. 1 (inset) with $n = 5$ and a load resistance $R_L = 100$ kΩ, in order to meet the following specifications:

- Attenuation smaller than 3 dB for frequencies up to $f_1 = 10$ Hz.
- Attenuation larger than 20 dB for frequencies beyond $f_2 = 500$ Hz.

In view of (1) with $n = 5$, it follows that $Y(s) = 5sC/(5sRC + 4)$. Therefore, the transfer function from the current source to the load current is given by

$$\frac{I_L(s)}{I_S(s)} = \frac{1}{1 + Y(s)R_L} = \frac{sRC + 0.8}{s(R + R_L)C + 0.8} \tag{2}$$

By using (2), it can be seen that the specifications are met by taking, for instance, $R = 1$ kΩ and $C = 30$ nF. For this choice of values, the attenuations at 10 Hz and 500 Hz are 0.2 dB and 21 dB, respectively. However, Fig. 4a shows that the specifications may be violated in the presence of random faults, which were simulated as in Section 3. Therefore, one should take the possible fault effects into account when designing the filter. For this purpose, let the admittance of the proposed circuit be represented as

$$Y(j2\pi f) = R^{-1} Y_p(j2\pi fRC) = R^{-1} A_p(fRC) \exp\left(j\phi_p(fRC)\right) \tag{3}$$

with $A_p(f)$, $\phi_p(f)$ denoting the amplitude and phase of the prototype admittance at frequency f, respectively. The filter attenuation L (in dB) is then expressed as

$$L_{dB}(f) = 20 \log_{10}\left[1 + R^{-1} A_p(fRC) R_L \exp\left(j\phi_p(fRC)\right)\right] \tag{4}$$

Let $(\underline{A}_p, \overline{A}_p)$ and $(\underline{\phi}_p, \overline{\phi}_p)$ denote the (lower, upper) amplitude quantiles obtained in Section 3 and the corresponding phase quantiles. The fault-tolerant design procedure adopted herein consists in choosing R, C to minimize a cost function $J(R, C)$ defined as

$$J(R,C) = \max\left\{ -3 + L_{dB}(f_1)\Big|_{A_p,\phi_p},\ 20 - L_{dB}(f_2)\Big|_{A_p,\phi_p};\ A_p = \underline{A}_p, \overline{A}_p,\ \phi_p = \underline{\phi}_p, \overline{\phi}_p \right\} \tag{5}$$

The notation $|_{A_p,\phi_p}$ with $A_p = \underline{A}_p,\ \overline{A}_p,\ \phi_p = \underline{\phi}_p,\ \overline{\phi}_p$ is used in (5) to indicate the evaluation of the filter attenuation at each combination of lower and upper quantiles for the amplitude and phase of the prototype admittance. If $J(R, C)$ is positive, it will correspond to the largest violation (in dB) of the design specifications. Therefore, the goal consists in obtaining a negative cost value, which should be decreased as much as possible in order to obtain suitable robustness margins.

The cost was evaluated over a grid spanning two decades of R, C values around the initial design (1 kΩ, 30 nF), with 20 logarithmically spaced points per decade. A minimum of -1.6 dB was obtained with $R = 2.5$ kΩ, $C = 53$ nF, which resulted in the frequency response shown in Fig. 4b. As can be seen, the specifications were met in all the 1000 Monte Carlo runs.

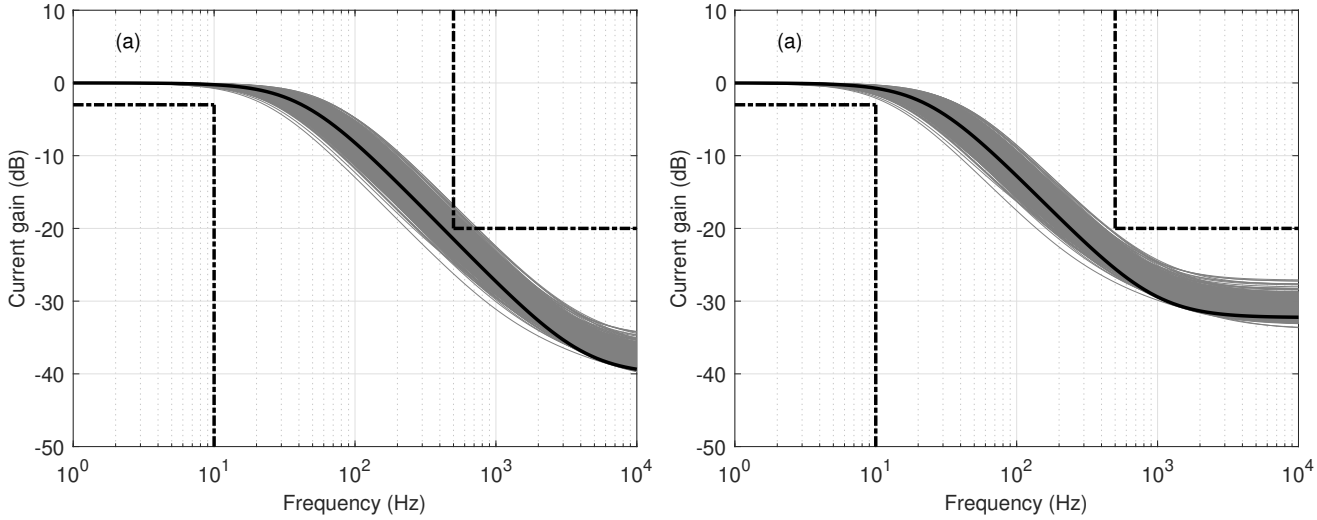

Figure 4: Frequency response of the low-pass filter in the presence of multiple faults at random locations (1000 Monte Carlo runs): (a) initial design and (b) fault-tolerant design. The thick black line and the dash-dotted lines correspond to the nominal response and the specification boundaries, respectively.

5 Conclusion

This paper proposed a two-dimensional RC network topology that can be used as a building block for the design of fault-tolerant circuits. The proposed topology does not have any single point of failure, in that no isolated short/open fault in an individual component can compromise the integrity of the circuit. Moreover, the network was shown to be robust to faults in several components simultaneously, with only minor deviations from the nominal frequency response (up to 3.9 dB in magnitude and 12.5° in phase in 95 % of the cases). In order to account for the effect of possible faults in subsequent design procedures, a statistical characterization of these deviations was carried out from the result of Monte Carlo simulations. In an illustrative example involving the design of a low-pass filter, this statistical characterization was exploited to choose suitable R, C component values through a simple grid search procedure. As a result, the filter specifications were met even in the presence of faults.

Future research may exploit the inclusion of inductive elements in the network, in order to achieve greater flexibility in the shaping of the admitance profile. This possibility is currently under investigation.

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Conflict of interest

The authors declare no conflict of interest.

Data availability statement

The MATLAB® code employed in this work is available from the authors upon request.

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