

(21) Application No: 0921638.3  
(22) Date of Filing: 30.05.2008  
(30) Priority Data:  
(31) 0710377 (32) 31.05.2007 (33) GB  
(86) International Application Data:  
PCT/GB2008/001821 En 30.05.2008  
(87) International Publication Data:  
WO2008/145995 En 04.12.2008

(71) Applicant(s):  
The University of Reading  
(Incorporated in the United Kingdom)  
Po Box 217, Whiteknights House, READING,  
RG6 6AH, United Kingdom  
(72) Inventor(s):  
James Arthur Dean Wallace Anderson  
(74) Agent and/or Address for Service:  
Barker Brettell LLP  
138 Hagley Road, Edgbaston, BIRMINGHAM,  
B16 9PW, United Kingdom

(51) INT CL:  
G06F 15/82 (2006.01)  
(56) Documents Cited by ISA:  
US 5761523 A US 5561804 A  
US 20040250046 A1  
GRAFE V G ET AL: "Implementation of the epsilon  
psilon dataflow processor" 19900102; 19900102 -  
19900105, vol. i, 2 January 1990 (1990-01-02), pages  
19-29.  
WEISS S ET AL: "ARCHITECTURAL IMPROVEMENTS  
FOR A DATA-DRIVEN VLSI PROCESSING ARRAY"  
JOURNAL OF PARALLEL AND DISTRIBUTED  
COMPUTING, ELSEVIER, MSTERDAM, NL, vol. 19, no.  
4, 1 December 1993 (1993-12-01), pages 308-322.  
YIJUN LIU ET AL: "The Design of a Dataflow  
Coprocessor for Low Power Embedded Hierarchical  
Processing" INTEGRATED CIRCUIT AND SYSTEM  
DESIGN. POWER AND TIMING MODELING, OPTIM  
IZATION AND SIMULATION LECTURE NOTES IN  
COMPUTER SCIENCE; LNCS, SPRINGER, BERLIN,  
vol. 4148, 1 January 2006, pages 425-438.  
(58) Field of Search by ISA:  
INT CL G06F  
Other: EPO-Internal

(54) Abstract Title: **Processors**

(57) A processing apparatus comprises a plurality of processors (12), each arranged to perform an instruction, and a bus (20) arranged to carry data and control tokens between the processors. Each processor (12) is arranged, if it receives a control token via the bus, to carry out the instruction, and on carrying out the instruction, to perform an operation on the data, to identify any of the processors (12) which are to be data target processors, and to transmit output data to any identified data target processors, to identify any of the processors which are to be control target processors, and to transmit a control token to any identified control target processors.

